15.3 A 390MHz Single-Chip Application and Dual-Mode Baseband Processor in 90nm Triple-V_t CMOS

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Presently, cellular phones are used not only for voice communications, e-mail, and web browsing, but also for more advanced functions such as video telephony and 3D Java games. Therefore, a high performance application processor, for example SH-Mobile [1], is typically embedded in a cellular phone in addition to a baseband processor. SH-MobileG1 (G1) achieves single-chip integration of an application and a baseband processor with a 20 power domain design that contributes to chip-set cost reduction and leakage power saving [2]. SH-MobileG2 (G2) is a second generation design comprised of a single-chip application and baseband processor, with a more sophisticated design in terms of both performance and power dissipation.

The design highlights of G2 are as follows:
(1) Triple-V_t technology in low-power 90nm CMOS achieves 390MHz for two CPUs in the application processor. This is 25% higher compared with 312MHz in G1 using the same process.

(2) To reduce the leakage power, the lowest-V_t cells are only used in the logic part of these two CPUs and a 3D graphics accelerator running up to 130MHz. Each of these three blocks is assigned to an independent power domain and can be powered-off when unused. G2 introduces a CPU core standby mode for these two CPUs, where caches and RAMs are powered and the logic part is shut-off.

(3) To reduce the dynamic power, a dynamic clock-stop scheme is introduced. The clock supply for bus-routers and bus-bridges are automatically stopped when no bus transaction is in progress.

(4) To enhance the performance of media IPs, 512KB media-RAM can be split up into 32 interconnect buffer (ICB) pieces, which act as read fill buffers, write-back buffers, or interconnect buffers through the ICB controller. 37% of the external SDRAM accesses can be saved in a VGA recording scenario and 30fps VGA quality can be achieved by using the ICB function.

Figure 15.3.1 shows G2 chip features. G2 integrates a total of 249M transistors, 14.8M gates and 31.0Mb memory. The die size is 11.15×11.15mm^2. In the application portion of the design, powerful media engines are integrated. A video processing unit (VPU) supports both MPEG4 and H.264 and a camera-IF with image processing unit handles up to 8Mpixel cameras. The baseband part has support for a dual-baseband system. A WCDMA block supports HSDPA service whereas the GSM block supports EDGE mode. Furthermore, G2 provides WCDMA/GSM voice handover function. Video telephony and motion picture play scenes consume 114mA and 73mA, respectively.

The power domain view of G2 is shown in Fig. 15.3.2. A total of 23 hierarchical power domains are defined to provide the useful power down control for the unused domains. The application part and baseband part are divided into 13, 8 power domains respectively with two additional common power domains (C4, C5). Clock buffers, repeater cells, hardware back-up FFs and a system controller are placed in the C5 domain whose power is always on. G2 introduces some power domains corresponding to distinguished functions, such as 3D graphics accelerator (A2RG), global positioning system (A4GP), and music play (A4MP), so that they can be powered-on only when the corresponding function is necessary.

Figure 15.3.3 shows the CPU and bus architecture. G2 consists of 3 CPUs, each of which runs a different OS. Therefore, the G2 system architecture supports multiple OS on heterogeneous multi-CPU cores. In the application part, an ARM1136 handles application system control and SHX2 plays a role in realtime media applications. In the baseband part, an ARM926 controls the baseband IPs including DSPs that accelerate the modem protocol handling. Every CPU can access any module of the chip as onchip buses are interconnected through bus bridges. In order to achieve high memory access performance, G2 provides 2 DDR controllers for separate DDR-SDRAMs.

A clock frequency of up to 390MHz is achieved for SHX2 and ARM1136 by using leaky transistors. As shown in Fig. 15.3.4, a CPU core standby mode is introduced with separate power domains for logic and RAM areas inside the CPU to reduce the static power dissipation. The CPU enters into core standby mode from the idle state by software control. In this mode, the power supply for the logic domain goes off and the VSS level of the RAM domain is raised to ARVSS level by an adjustment circuit. The leakage power is reduced to 0.04mA, compared to 1.28mA for the sleep mode, where only the clock supply is stopped. As the data in RAMs and caches are retained during the core standby mode, the CPU can resume the operations quickly when waking-up from this mode. Transition time and recovery time to and from this mode including time for saving and retrieving of hardware resources by software is as small as 5μs and 7μs, respectively. The sleep-mode of G1 can be replaced by the core standby mode in G2.

G1 supports a module standby mode to stop the clock supply for an unused module. In addition to this software clock supply control, G2 introduces a dynamic clock-stop scheme. The dynamic clock-stop scheme is mainly adopted for onchip bus-router and bus-bridge modules. As shown in Fig. 15.3.5, a clock-driver supplying clock for a module-level is gated by hardware logic during a period of no bus transaction. When a new bus request is detected by the logic, the clock-driver starts the clock supply automatically. Two-cycle bus latency is added for a bus request that arrives during a clock-stop condition. The module provides a programmable counter to specify when to stop the clock supply after one bus transaction is completed. No additional latency is inserted for continuous bus transactions by programming the counter with the appropriate value. This scheme cuts dynamic power consumed by these modules to nearly 0 when no bus transaction is required, while G1 consumes dynamic power that may be as much as 30mA in these modules.

Each of the Media-IPs of G1 needs external SDRAM accesses for all input and output data. G2 introduces interconnect buffers (ICB) shown in Fig. 15.3.6 to enhance the performance of motion picture processing. The ICB controller is located between RT-SHwy bus router and 13 media-IPs, and controls 512KB embedded media-RAM (MERAM). MERAM can be configured as up to 32 small ICB pieces. Each media-IP can use one or more ICBs as read fill buffers and write-back buffers. Multiple complicated accesses from media-IPs are buffered in ICBs and are re-ordered in simple line-type accesses from/to the external SDRAM. ICB can also be used as an interconnect buffer, where one media-IP writes to the ICB and another media-IP receives the data via the ICB. In one scenario of VGA recording, 37% of external SDRAM accesses are replaced with on-chip MERAM accesses by using the ICB function. Figure 15.3.6 also shows the details of VPU. It handles both MPEG-4 and H.264 with dedicated operational units by pipelined control. By utilizing the VPU and ICB function, 30fps VGA-quality video is achieved.

References:
[1] T. Kamei, et al., "A Resume-Standby Application Processor for 3G Cellular Phones," *ISSCC Dig. Tech. Papers*, pp. 336-337, Feb., 2004.
[2] T. Hattori, et al., "A Power Management Scheme Controlling 20 Power Domains for a Single-Chip Mobile Processor," *ISSCC Dig. Tech. Papers*, pp. 542-543, Feb., 2006.

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Die size	11.15 × 11.15mm^2
Process	90nm LP, CMOS triple-V_t, 8M(7Cu+1Al)
CPU	AP-Realtime: SHX2, 390MHz AP-System: ARM1136JF-S, 390MHz Baseband: ARM926EJ-S, 130MHz
Application Part	VPU(MPEG4/H.264), VIO(up to 8M pixel camera), 3D Graphics Accelerator, 512KB-Media-RAM(MERAM), GPS
Baseband Part	Dual Baseband (WCDMA with HSDPA, GSM/GPRS/EDGE)
# of Power Domains	23 (2 for Common, 13 for Application, 8 for Baseband)
Supply voltage	1.2V(internal), 1.8/2.5/3.3V(I/O)
Power Dissipation (1.2V domain)	(1) Video Telephony (w/o noise canceling, w/o echo canceling): 114mA MPEG-4 codec QCIF 15fps 64kb/s, AMR codec (2) Motion Picture Play: 73mA MPEG-4 decode QVGA 30fps 384kb/s, AAC decode 128kb/s 48kHz
I/O	617 pins
# of TRs (gates, memory)	249.3M TRs (18.4M gates, 25.0Mb RAM, 6.0Mb ROM)

Figure 15.3.1: Chip Features.

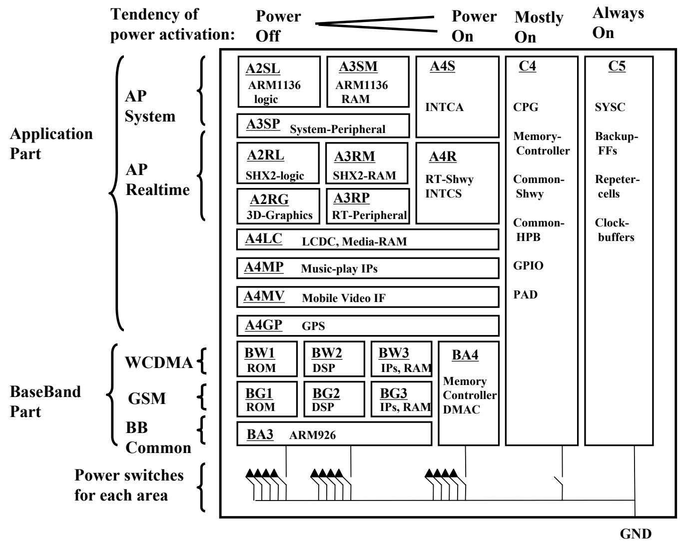

Figure 15.3.2: Power Domain View.

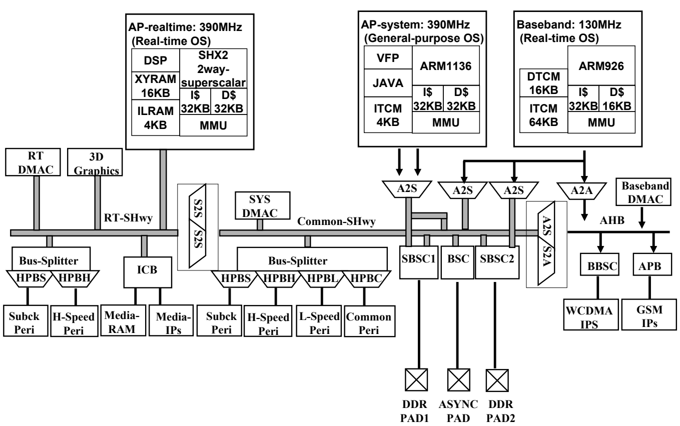

Figure 15.3.3: CPU and Bus Architecture.

CPU Power-mode	Normal	Sleep	Core Standby	Power Off
Clock	On	Off	Off	Off
Power supply for Logic	On	On	Off	Off
Power supply for RAM	On	On (Resume)	On (Resume)	Off
Transition Time to the Mode	-	1.0μs	5.0μs	> 20μs(*1)
Recovery Time from the Mode	-	1.0μs	7.0μs	> 40μs(*2)
Leakage power of SHX2 area (*3)	1.71 mA	1.28 mA	0.04 mA	0.00 mA

(*1) Including dirty cache line write-back (*2)Including cache and RAM refill
(*3) Simulated in process-worst at room temperature

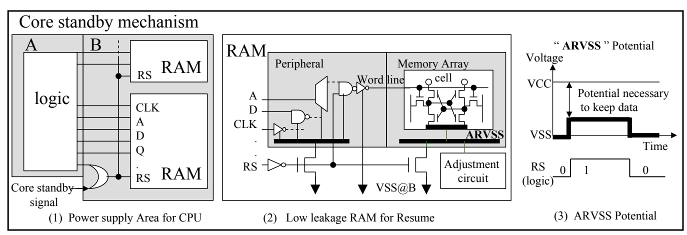

Figure 15.3.4: CPU Core Standby Mode.

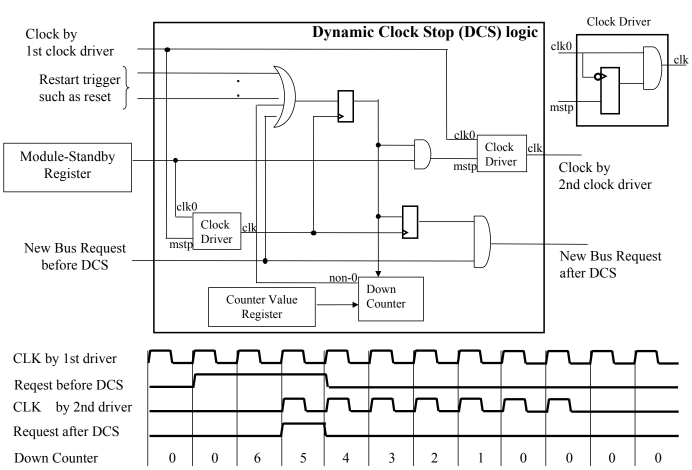

Figure 15.3.5: Dynamic Clock Stop Scheme.

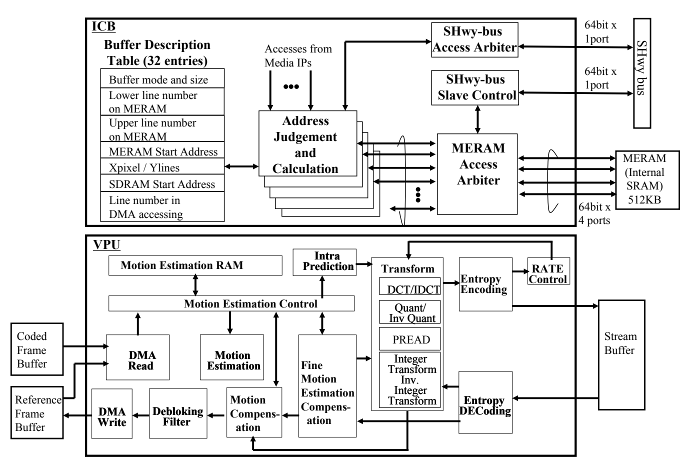

Figure 15.3.6: Video Processing Unit (VPU) and InterConnect Buffers (ICB).

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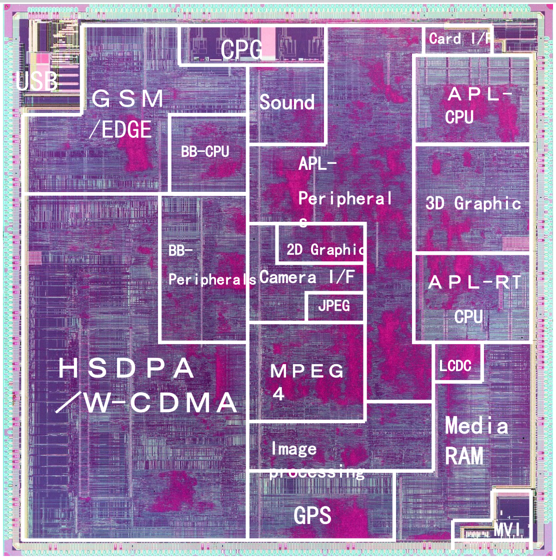

Figure 15.3.7: SH-MobileG2 Die Micrograph.